REMARKS

Claims 1-27 and 29-68 are all the claims pending in the application.

Support for the amendment of claim 25 may be found in the specification as originally filed, for example, in the originally filed claims, and page 58, line 29 to page 59, line 28 of the specification. Claims 26, 32 and 65 are amended in accordance with the amendment of claim 25.

Support for the amendment of claim 30 may be found in the specification as originally filed, for example, in the originally filed claims, and page 59, line 35 to page 60, line 6 of the specification.

Claim 31 is amended to clarify the constitution of the multilayer printed circuit board according to the present invention. Support for the amendment of claim 31 may be found in the specification as originally filed, for example, in the originally filed claims, and page 55, lines 18 to 21 of the specification.

Support for the amendment of claim 64 may be found in the specification as originally filed, for example, at page 40, lines 3 to 4 of the specification.

I. The Objection to Claims 64 and 66

The Examiner objects to claims 64 and 66 as allegedly containing "informalities."

Claim 64 has been amended for clarity and to recite the complete terms therein. Claim 66 has been canceled.

It is respectfully submitted that Applicants' claims are clear and definite and it is requested that the objection to claim 64 be reconsidered and withdrawn.

II. The Rejection under 35 U.S.C. §112, first paragraph

Claim 65 and 66 are rejected under 35 U.S.C. §112, first paragraph, as allegedly failing to comply with the written description requirement.

Applicants respectfully submit that the specification as originally filed describes the claimed subject matter of claim 65 in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. See, for example, page 57, lines 19-21 of the specification. Claim 66 has been canceled. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the rejection under 35 U.S.C. §112, first paragraph.

III. The Rejection under 35 U.S.C. §112, second paragraph

Claims 25-27, 29-32 and 64-66 are rejected under 35 U.S.C. §112, second paragraph, as allegedly being indefinite.

Applicants request that the Examiner reconsider and withdraw the rejection under 35 U.S.C. §112, second paragraph, in view of the following remarks.

Claims 25 and 30 have been amended to clarify the language and to more particularly point out and distinctly claim Applicants' invention.

Claim 25 is amended to clarify the constitution of the multilayer printed circuit board according to the present invention. Claim 25 clearly recited that thermosetting polyolefin resin is the material of the resin insulating layers. Further, claim 25 clearly recites that the lower metal layer and the conductor circuit are separate elements.

Claim 30 is amended to clarify the constitution of the multilayer printed circuit board according to the present invention. Claim 30 clearly recites that each of the conductor circuits has an upper metal layer on its surface. The material of the upper metal layer is also now clearly recited.

For clarity, the resin insulating layers of claim 25 are designated "first" resin insulating layers and the resin insulating layer of claim 30 is designated a "second" resin insulating layer. Claim 25 recites a resin substrate board carrying, on both sides thereof, "first" resin insulating layers. Each of the first resin insulation layers has a lower metal layer and then a conductor circuit thereon. Claim 30 further recites the presence of an upper metal layer, and that the upper metal layer may have a "second" resin insulating layer built thereon. Therefore, claim 30 relates to a resin insulating layer that is not one of the resin insulating layers of claim 25. However, Applicants note that in some embodiments, some of the first resin insulating layers and the second resin insulation layer may be "labeled" or described as a "interlayer" resin insulating layer. An interlayer resin insulation layer is a resin insulating layer placed above a conductor circuit and below another conductor circuit. See, for example, Example 23 in Applicants' specification, by repeating a sequence of steps (8) to (15) (page 147, lines 34 to 35), resin insulating layers are formed, one after another, above previously-formed resin insulating layers. These resin insulating layers function as interlayer resin insulating layers of the multilayer printed circuit board. Applicants' specification, page 58, lines 5 to 7.

New dependent claims 67 and 68 further recite that the multilayer printed circuit board may comprise successive series of insulating, metal layer, conductor circuits.

For the above reasons, it is respectfully submitted that Applicants' claims are clear and definite and it is requested that the rejection under 35 U.S.C. §112 be reconsidered and withdrawn.

IV. Brief Summary of Applicants' Invention

Prior to specifically addressing the Examiner's rejections, Applicants have prepared the following summary of the present invention to assist the Examiner in understanding Applicants' claimed invention.

The present invention discloses a " multilayer printed circuit board comprising:

a resin substrate board having, on both sides thereof, first resin insulating layers each comprised of the same resin material;

a lower metal layer, having a conductor circuit made of metal and having the same pattern as said lower metal layer, on each of said first resin insulating layers; and

wherein

said resin insulating layers comprise thermosetting polyolefin resin; and

said lower metal layers are composed of at least one metal selected from among metals (exclusive of Cu) of the 4^{th} through 7^{th} periods in Group 4A through Group 1B of the long-form periodic table of the elements, Al, and Sn" (claim 25).

A multilayer printed circuit board having a resin insulating layer and a conductor circuit made of metal generally has a problem that the metal comprised in the conductor circuit and the resin insulating layer under the conductor circuit have a poor adhesion. In order to insure a good adhesion, the surfaces of the resin insulating layer and conductor circuit are roughened in the

conventional manufacturing process. Incidentally, the above-mentioned conductor circuit is mostly comprised of metal, and does not comprise a resin.

Recently it is required to handle a multilayer printed circuit board with high frequency signals. Since the surfaces of the resin insulating layer and the conductor circuit are roughened, the carrying of high frequency signals tends to be followed by a signal conduction noise attributable to the surface irregularities.

This problem is particularly conspicuous when the resin has a low dielectric constant and a low dielectric loss tangent. In the event such a resin is used for a resin insulating layer, the multilayer printed circuit board according to the present invention employs the following constitution in order to solve the above problem.

First, a metal layer comprising at least one metal recited in claim 25, which has a good adhesion with a resin, is formed on a resin insulating layer. Then a conductor circuit, such as a metal layer comprising Cu and the like, is formed on the first metal layer. Namely, two layers, a lower metal layer and a conductor circuit layer, are formed on the resin insulating layer. Since the lower metal layer has a good adhesion with the resin insulating layer, there is no need to roughen the surfaces of the resin insulating layer and the conductor circuit. The conductor circuit does not have surface irregularities. Therefore, the above-mentioned signal conduction noise attributable to the surface irregularities is suppressed even when high frequency signals are carried.

V. **The Rejection Under 35 U.S.C. §102 Based on Oodaira et al**

Claims 25-27, 29, and 64-66 are rejected under 35 U.S.C. §102(b) as allegedly being anticipated by Oodaira et al (US Patent No. 4,7151,126).

Applicants respectfully submit that the present invention is not anticipated by or obvious over the disclosures of Oodaira et al and request that the Examiner reconsider and withdraw this rejection in view of the following remarks.

Oodaira et al discloses a circuit board comprising a plurality of resin substrates and at least one circuit pattern of a conductive resin.

The circuit pattern 83 of Oodaira et al is different in constitution from the conductor circuit of the present invention. The conductor circuit of the present invention has a metal layer. On the other hand, the circuit pattern 83 of Oodaira et al comprises a conductor resin composition (col. 9, line 31 to 33). The resistivity of such a circuit pattern is higher than that of a circuit pattern comprising metal only. Therefore, the electrical conductivity of such a circuit pattern is very much inferior to that of a circuit pattern comprising metal only. In particular, when a complex and minute circuit pattern having a small cross-sectional area is formed by a conductor resin composition, it does not function as a conductor circuit.

It should also be noted that the circuit pattern 83 of Oodaira et al has a good adhesion with the resin substrates since it comprises a conductor resin composition. In Oodaira et al, a conductor resin composition is required since the circuit pattern is formed by thermocompression and deformation so that electrical connections between the upper and lower circuit patterns is achieved (Example 7). Accordingly, one of ordinary skill in the art would learn nothing from

Oodaira et al about the problem that a conductor circuit mostly comprised of metal and a resin insulating layer under the conductor circuit have a poor adhesion.

On the other hand, as discussed above, the conductor circuit of the present invention has a metal layer which has a poor adhesion with the resin insulating layer. The present invention is completely different in concept from Oodaira et al. Oodaira et al offer no motivation to one of ordinary skill in the art to achieve the present invention.

Further, since Oodaira et al does not teach or even suggest about the adhesion problem, one of ordinary skill in the art would not think to construct two metal layers, the lower metal layer and the conductor circuit layer, on the resin insulating layers in order to solve the problem. Needless to say, Oodaira et al does not teach or suggest about construction of two metal layers. The circuit patterns illustrated in Fig. 7 have only one layer comprising a conductor resin composition.

As discussed above, the multilayer printed circuit board according to the present invention is different in constitution, especially in constitution of the conductor circuit, from the circuit board according to Oodaira et al. Therefore, the present invention is not anticipated by Oodaira et al.

Further, since there is no possibility that the adhesion problem occurs in Oodaira et al, Oodaira et al offers no motivation to one of ordinary skill in the art to achieve the present invention. Accordingly, the present invention is not obvious from Oodaira et al.

Since the subject matter of independent claim 25 is neither taught by nor obvious from Oodaira et al, it is respectfully submitted that the rejection of claim 25 and claims 26, 27, 29, 64 and 65 depending from claim 25 under 35 U.S.C. §102(b) be reconsidered and withdrawn.

VI. The Rejection Under 35 U.S.C. §103 Based on Oodaira et al in view of Brandli et al

Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oodaira et al in view of Brandli et al (US Patent No. 5,227,012).[1]

Applicants respectfully submit that the present invention is not obvious over the disclosures of Oodaira et al and Brandli et al and request that the Examiner reconsider and withdraw this rejection in view of the following remarks.

Brandli et al discloses a multi-layer thin film circuit containing an integrated thin film vesistor. The purpose of Brandli et al is to manufacture the integrated thin film resistor comprising precisely arranged resistors which can be utilized in constructing various devices. On the other hand, the multilayer printed circuit board according to the present invention is used to mount IC and LSI on it. Therefore, Brandli et al and the present invention are different in use of the product.

According to Brandli et al, an adhesion layer 1' is formed on an insulating layer 5, and a conductor film 2' is formed on the adhesion layer 1'. The adhesion layer 1' is formed of an oxidation-prone metal such as Cr, Ti, and W, and the conductor film 2' is formed of Cu, Ni or the like (Brandli et al, col. 3, lines 52 to 57). The above constitution is only generally similar to the

[1] The Examiner is requested to clarify this rejection. Claim 31 is not listed as a rejected claim, but is discussed in paragraph 9 (Office Action, top of page 8).

constitution recited in claim 25 of the present invention. For example, the insulating layer 5 is formed of negative photo-sensitive polyimide (Brandli et al col. 4, lines 3 to 4) which is a conventional material. Brandli et al does not teach to use thermosetting polyolefin resin, which is used in the present invention.

Further, Brandli et al uses a ceramic substrate S (Brandli et al, col. 3, line 51). A ceramic substrate hardly has a mechanical warp. Further, the adhesion layers 1 and 1', the conductor films 2 and 2', and the conductor tracks 3 and 3' are all formed on one side of the thick ceramic substrate S. Therefore, it is unlikely that peeling of the conductor circuit, attributable to a lack of adhesion, occurs in Brandli et al.

Moreover, it is not explicitly described in Brandli et al that the surface of the insulating layer on which a conductor circuit is formed is flat. It is highly possible that a roughening treatment is performed on the insulating layer in order to improve the adhesion.

Accordingly, even though the multi-layer thin film circuit of Brandli et al comprises metal layers, adhesion layer 1' and conductor film 2' , on the insulating layer 5, the effect of the present invention cannot be foreseen from Brandli et al. In other words, it cannot be foreseen from Brandli et al that a good adhesion is maintained and the above-mentioned peeling is prevented when a lower metal layer is provided on each of resin insulating layers, comprising thermosetting polyolefin resin, located on both sides of a thin resin substrate board.

Therefore, even if the disclosures of Oodaira et al and Brandli et al are combined, the present invention would not have been obvious to one of ordinary skill in the art.

As discussed above, the multilayer printed circuit board of the present invention is different in constitution from the multi-layer thin film circuit of Brandli et al. Further, the present invention is not obvious from Brandli et al.

The rejection of claim 30 under 35 U.S.C, §103 (a) as being unpatentable over Oodaira et al in view of Brandli et al is respectfully traversed since Brandli et al fails to remedy the deficiency of Oodaira et al.

According to the present invention, an upper metal layer is formed between the conductor circuit and the resin insulating layer. On the other hand, according to Brandli et al, the insulating layer 5 is formed directly on the conductor track 3 or 3'. In view of the teachings of Oodaira et al and Brandli et al, the multilayer printed circuit board as recited in claim 30 would not have been obvious to one skilled in the art.

The rejection of claim 31 is also respectfully traversed.

The Examiner indicates that it would have been obvious to one of ordinary skill in the art to combine Oodaira et al and Brandli et al in order to construct a lower metal layer, a Cu layer, and a conductor circuit on a resin insulating layer.

However, as discussed above, Oodaira et al does not teach or even suggest the adhesion problem. The circuit pattern 83 of Oodaira et al has a good adhesion with the resin substrates in the first place, since it comprises a conductor resin composition. Therefore, there is no motivation to combine Oodaira et al and Brandli et al to construct a lower metal layer, a Cu layer, and a conductor circuit on a resin insulating layer in order to maintain a good adhesion.

For the above reasons, it is respectfully submitted that the subject matter of claims 30 and 31 is neither taught by nor made obvious from the disclosures of Oodaira et al and Brandli et al, either alone or in combination, and it is requested that the rejection under 35 U.S.C. §103(a) be reconsidered and withdrawn.

VII. The Rejection Under 35 U.S.C. §103 Based on Oodaira et al

Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oodaira et al.

Since the subject matter of independent claim 25 is neither anticipated by nor obvious over Oodaira et al as discussed above, it is respectfully submitted that the rejection of dependent claim 32 under 35 U.S.C. §103(a) is not obvious over Oodaira et al for the same reasons.

For the above reasons, it is respectfully submitted that the subject matter of claims 32 is neither taught by nor made obvious from the disclosures of Oodaira et al and it is requested that the rejection under 35 U.S.C. §103(a) be reconsidered and withdrawn.

VIII. Conclusion

In view of the above, Applicants respectfully submit that their claimed invention is allowable and ask that the objections to the claims, the rejections under 35 U.S.C. §112, the rejection under 35 U.S.C. §102 and the rejections under 35 U.S.C. §103 be reconsidered and withdrawn. Applicants respectfully submit that this case is in condition for allowance and allowance is respectfully solicited.

If any points remain at issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the local exchange number listed below.

Applicants hereby petition for any extension of time which may be required to maintain the pendency of this case. The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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